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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,758	09/12/2003	Yu-Fang Wang	048747-0203	8155
23392	7590	12/12/2005	EXAMINER	
FOLEY & LARDNER 2029 CENTURY PARK EAST SUITE 3500 LOS ANGELES, CA 90067			KIM, RICHARD H	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/661,758

Applicant(s)

WANG, YU-FANG

Examiner

Richard H. Kim

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 October 2005.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-29 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/3/05 has been entered.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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2. Claims 1-4, 8-10, 12-15, 19-21, 23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagata et al. (US 6,118,005).

Referring to claims 1, 26 and 27, Nagata et al. discloses a method comprising providing a substrate (1); forming respective gate lines (2) and signal lines (13) on the substrate, wherein the plurality of gate line and signal lines define respective pixel areas (14); forming a plurality of switching elements (5) electrically connected to the signal line and gate lines for the pixel areas; forming a protruding pattern (14) on the gate line, the signal lines, and the switching elements to define respective color filter unit areas (14); applying color resin to form respective color filter units in the color filter unit areas defined by the protruding pattern (col. 4, lines 55-60); the respective color filter units having respective top surface with edge portions that are planar and are at the same height with respective edge portions of a top surface of the protruding pattern (Fig. 2); and forming respective pixel electrodes (15) on the respective top surfaces of the respective color filter units and on the respective edge portions of the top surface of the protruding pattern.

Referring to claims 12, 28 and 29, Nagata et al. discloses a device comprising a substrate (1); a pixel matrix comprising of a plurality of gate line (2) and signal lines (13) to define respective pixel areas (14); respective switching elements (5) for each of the pixel areas electrically connected to the signal lines and gate lines; a protruding pattern (14) formed on the gate lines, the signal lines, and the switching elements and defining respective color filter unit areas; respective color filter units (14R, 14G, 14B) formed in the respective color filter unit areas, the respective color filter units having respective top surfaces with edge portions that are planar and at a same height with respective edge portions of a top surface of the protruding

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pattern; and respective pixel electrodes (15) formed on the respective top surfaces of the respective color filter units and on the respective edge portions of the top surface of the protruding pattern.

Referring to claims 2 and 13, Nagata et al. discloses that the substrate is an insulator (1).

Referring to claims 3 and 14, Nagata et al. discloses that the switching elements are thin film transistors (6).

Referring to claims 4 and 15, Nagata et al. discloses that the protruding pattern is made of organic material (col. 5, lines 10-11).

Referring to claims 8 and 19, Nagata et al. discloses that the protruding pattern is patterned by photolithography and consists of a photoresist material (Fig. 3).

Referring to claims 10 and 21, Nagata et al. discloses that the pixel electrodes are substantially made of transparent conductive materials (15).

Referring to claim 23, Nagata et al. discloses a gate electrode extending from a gate line (2); a gate insulating layer (4) formed on the gate electrodes; and a pair of source and drain electrodes (12, 13) formed on the gate insulating layer above the gate electrode to form a thin film transistor (7).

Referring to claims 9 and 20, Nagata et al. discloses the device wherein the gate lines and the signal lines are substantially made of opaque conductive materials (col. 8, line 55).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. in view of Takizawa et al. (US 6,573,964 B1).

Nagata et al. discloses the device and method previously recited. Nagata et al. further discloses that the protruding pattern is made of carbon black (col. 6, lines 5-6). However, the reference does not disclose that the protruding pattern further includes polyimide and novolak resin.

Takizawa et al. discloses an insulating layer made of novolak and polyimide (col. 11, lines 53-64).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the protruding pattern to further include polyimide and novolak resin since one would be motivated to utilize an effective material capable of dividing two different areas of a liquid crystal display (abstract).

5. Claim 6, 7, 11, 17, 18, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. in view of Sato et al. (US 5,919,532).

Referring to claims 6, 7, 17 and 18, Nagata et al. discloses the device previously recited, and further discloses that the pixel electrodes are electrically connected to corresponding switching elements via contact holes (Fig. 2, ref. 16), but fails to disclose that the protruding pattern comprises respective contact holes exposing parts of the corresponding switching elements.

Sato et al. discloses a device wherein the protruding pattern comprises respective contact holes exposing parts of the corresponding switching elements (Fig. 2, ref. 2').

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ protruding pattern comprises respective contact holes exposing parts of the corresponding switching elements since one would be motivated to further protect the TFTs with the protruding pattern (col. 23, lines 60-62).

Referring to claims 11 and 22, Nagata et al. discloses the device previously recited, but fails to disclose that the colored resin is applied by inkjet printing.

Sato et al. discloses a device wherein the colored resin is applied by inkjet printing (Fig. 5G).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the colored resin to be applied by inkjet printing since one would be motivated to provide a method of easily fabricating such an active matrix substrate (col. 6, lines 33-35).

Referring to claims 24 and 25, Nagata et al. discloses the device previously recited, and further discloses the method wherein the step of forming a plurality of switching elements electrically connected to the signal line and gate lines for the pixel areas comprises forming a plurality of gate electrodes connected to the gate lines (2); forming a first insulating layer on the plurality of gate electrodes (4); forming a plurality of source electrodes (13) and a plurality of drain electrodes (12) on the first insulating layer, the plurality of source electrodes being connected to the signal lines; and forming a second insulating layer on the plurality of source electrodes and the plurality of drain electrodes, the second insulating layer formed with

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respective conductive openings passing through the second insulating layer over respective drain electrodes of the plurality of drain electrodes (Fig. 2); and wherein the step of forming the protruding pattern on the gate lines, the signal lines and the switching elements to define respective color filter areas comprises forming a protruding pattern (14Black) on the gate line, the signal line and the switching elements to define respective color filter unit areas (11), comprises forming a protruding pattern (14 Black) on the gate lines, the signal lines and the switching elements to define respective color filter unit area (14R,G,B). However, the reference does not disclose the protruding pattern is formed with respective contact holes aligned with corresponding openings in the second insulating layer.

Sato et al. discloses a device wherein the protruding pattern is formed with respective contact holes aligned with corresponding openings in the second insulating layer (Fig. 2, ref. 2').

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the protruding pattern to be formed with respective contact holes aligned with corresponding openings in the second insulating layer since one would be motivated to further protect the TFTs with the protruding pattern (col. 23, lines 60-62).

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.



***Conclusion***

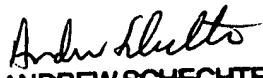
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard H. Kim whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard H Kim  
Examiner  
Art Unit 2871

RHK

  
ANDREW SCHECHTER  
PRIMARY EXAMINER

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